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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,257	10/03/2003	Satoshi Inoue	039282.03	9107

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,257	INOUE, SATOSHI	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed on January 13, 2006. Claims 1-32 were canceled. Claims 33-45 have been newly added.

Specification

1. Claim 40 is objected to because of the following informalities: In claim 40, line 5 and line 6, "first intrinsic parts" should apparently be --first impurity parts-- due to the first impurity portion being separated. Appropriate correction is required.

Duplication Objection

*** Claim 34 is duplicated that of claim 33 for covering the same things, since "the second impurity portion being separated into two parts by the intrinsic portion" in claim 34 is merely rephrased and already included in claim 33. Applicant is advised that should the claims be found allowable, the duplicated claims will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording. See MPEP § 706.03(k). One of the claims should be amended or cancelled to avoid the duplication.

Claim Rejections - 35 USC § 102

2. Claims 33-36,41-42,45-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (5,830,787).

Re claims 33-35, Kim teaches (at Figs 3b-3e,4d-4f; col 3-4) a method of manufacturing a transistor, comprising: forming a semiconductor film on a substrate; forming an intrinsic portion 43 (undoped polysilicon layer 43 ; col 3, lines 35-42) and a first impurity portion 50,52 in the semiconductor film by applying a first impurity atom to the semiconductor film (Figs 3c,3d,4e), the intrinsic portion 43 not including the first impurity atom, the first impurity portion including the first impurity atom; forming an insulator film 47 over the semiconductor film; forming a gate electrode 45 over the insulator film 47, the gate electrode 45 overlapping with at least a part of the intrinsic portion 43 and at least a part of the first impurity portion 50 (Fig 3c,4e); and forming a second impurity portion 52,53 in the semiconductor film by applying a second

impurity atom to the semiconductor film using the gate electrode 45 as a mask, the second impurity portion being separated into two parts 52,53 by at least the intrinsic portion 43. Re claim 36, wherein first impurity portion is being separated into at least two parts 50,52 by the intrinsic portion 43 by applying the first impurity atom to the semiconductor film (Figs 4e,3d). Re claim 41, further comprising: applying an energy to the semiconductor film to crystallize it (col 3, lines 17-22) before the forming of the intrinsic portion and the first impurity portion. Re claim 42, a dosage of the first impurity portion 52 being larger than a dosage of the second impurity portion 50 (col 3, lines 42-55). Re claim 45, wherein a display device is made by using the method of manufacturing a transistor (col 1, lines 16-22). Re claim 46, wherein an electronic apparatus is made by using the method of manufacturing a transistor (col 1, lines 16-22).

Claim Rejections - 35 USC § 103

3. Claims 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (5,830,787) taken with Kawashima et al (5,016,986).

Kim teaches (at Figs 3b-3e,4d-4f; col 3-4) a method of forming a transistor as applied to claims 33-36,41-42,45-46 above.

Kim already teaches the method of manufacturing the transistor and display device, but lacks using the method for manufacturing an active matrix substrate (claim 43), and an electroluminescent device (claim 44).

However, Kawashima teaches (at col 10, lines 60-68) applying the method in manufacturing a liquid crystal display as active matrix substrate, and other devices including a plasma display device, an electroluminescence display device, and electronic devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the method of manufacturing the transistor of Nakagawa or Okada in manufacturing other devices including the active matrix substrate as liquid crystal display, the electroluminescence display device, the plasma display device, and the electronic devices, as taught by Kawashima. This is because of the desirability to manufacture different and various types of devices by using transistors having high speed operation with lower power consumption.

4. Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (5,830,787) taken with Takemura et al (5,569935).

Kim teaches (at Figs 3b-3e,4d-4f; col 3-4) a method of forming a transistor as applied to claims 33-36,41-42,45-46 above.

Kim already teaches forming the gate electrode overlapping an intrinsic portion and a part of a first impurity regions, but lacking having two separated intrinsic parts and two separated impurity parts (re claims 37-40).

However, Takemura teaches (at Figs 1A-1C; 3A-3E; col 3, lines 41 through col 5) forming a transistor having a the intrinsic portion being separated into at least two parts by the first impurity portion, wherein the semiconductor film is having a channel region under the gate electrode, the channel region consisted of the intrinsic portion and the first impurity portion, the intrinsic portion being separated into a plurality of intrinsic parts and the first impurity portion being separated into a plurality of first intrinsic parts, the plurality of intrinsic parts and the plurality of first intrinsic parts being arranged in a channel width direction.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Kim by forming the intrinsic portion into a plurality of intrinsic parts and the first impurity portion into a plurality of first intrinsic parts, as taught by Takura. This is because of the desirability to form a plurality of transistors.

Response to Amendment

5. Applicant's remarks filed January 13, 2006 have been fully considered but they are moot in view of the new ground(s) of rejection.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-16

Michael Trinh
Primary Examiner